Homework Assignment 3
CIS501 Fall 2005

Due: Monday, October 24^{th} at 12:30pm.

Instructions: Your solution to this assignment must be type-written, except for the questions that you answer on the provided worksheet.

Question 1 (14 points):
Consider a 48-bit machine with 32KB pages and maximum 1GB of physical memory. Assume that each PTE contains a PPN only and that PTEs are an integer number of bytes (i.e., even if a PTE is 9 bits, it is stored as 2 bytes).

(a). (7 points) How much storage is needed for a single-level page table?

(b). (7 points) How much storage is needed for the first-level table only of a two-level physical page table? (Assume the first level table holds full physical addresses and each 2nd level table is 32KB in size)

(c). (extra credit: 1 point) How might you reduce the size of each entry in the first-level table in part (b) without changing the structure of second-level page table?

Question 2 (14 points): A disk has a rotational speed of 6000 RPM, a seek time of 15ms, and negligible controller overhead. Each track has 256 sectors and each sector is 512B. The disk is connected to memory via an I/O bus capable of transferring 4MB/s data. The disk contains a cache to buffer in-flight data, and this cache allows the disk to overlap data transfer over the I/O bus with the next disk access.

(a). (4 points) What is the maximum bandwidth of the disk? What is the minimum amount of time (in seconds) that a program could possibly scan 40MB of data transferred from the disk?

(b). (5 points) How long does it take to transfer 128KB data from disk to memory assuming the data is found sequentially on one track (assume the disk still must seek and rotate to find the start of the data)?

(c). (5 points) How long does it take to transfer 128KB data from disk to memory assuming the data is found in sectors which are randomly scattered across the disk?

Question 3 (22 points): Consider the following code:

```
0: ld [r1]→r5
1: add r5, 1→r5
2: ld [r1+4]→r6
3: cmplti r5, r6→r2
4: bne r2, 0, instruction#7
5: sub r5, 1→r5
6: ld [r1+8]→r6
7: st r6→[r1]
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(a). (3 points) Identify the data hazards (RAW, WAR and WAW). For each type of dependence (RAW, WAR and WAW), make a list of the dependencies of that type found in the above code. You would write each dependence in the list by stating the producer instruction number, the consumer instruction number, and the register in which the data is passed. For example, if instruction 0 produces a value which is consumed by instruction 2 in register r5, you write: "RAW: #0→#2 (r5)"

(b). (5 points) Consider a processor with a simple pipeline with stages F, D, X, M, W. The processor has full bypassing and is fully pipelined. Assume that the execution of every instruction takes 1 cycle and loads have the usual additional single-cycle delay for dependent operations. Assume the branch (instruction #4) is NOT taken and that it is correctly predicted. Complete the pipeline diagram showing the execution of the code on the processor. Please answer this question on the provided worksheet.

(c). (4 points) Consider a processor with a six-cycle pipeline due to a two-cycle data cache. The resulting pipeline has the stages F, D, X, M_1, M_2, W. In such a pipeline, loads have an additional delay cycle, resulting in a two-cycle delay for dependent operations. As in part (b), assume the branch (instruction #4) is NOT

taken and that it is correctly predicted. Complete the pipeline diagram showing the execution of the code on the processor. Please answer this question on the provided worksheet.

(d). (7 points) Reschedule the code to obtain the fastest instruction schdule for this code sequence for original five-cycle pipeline described in part (b). Again, assume the branch (instruction #4) is NOT taken and that it is correctly predicted. Complete the pipeline diagram showing the execution of your code. Please answer this question on the provided worksheet.

(e). (4 points) Consider the original code and processor from part (b). Assume the branch is not predicted NOT taken. However, unlike before, the branch is actually taken (resulting in a branch misprediction). The processor detects the branch misprediction during the X stage of the pipeline. Complete the pipeline diagram showing the execution of the code on the processor. Please answer this question on the provided worksheet.

Questions 3 Worksheet

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Name:

Question b:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
ld [r1]→r5	F	D	X	M	W															
add r5,1→r5																				
ld [r1+4]→r6																				
cmplti r5,r6→r2																				
bne r2,0,instruction#7																				
sub r5,1→r5																				
ld [r1+8]→r6																				
st r6→[r1]																				

Question c:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
ld [r1]→r5	F	D	X	M1	M2	W														
add r5,1→r5																				
ld [r1+4]→r6																				
cmplti r5,r6→r2																				
bne r2,0,instruction#7																				
sub r5,1→r5																				
ld [r1+8]→r6																				
st r6→[r1]																				

Question d:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

Question e:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
ld [r1]→r5	F	D	X	M	W															