Milo M. K. Martin

Curriculum Vitae

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Computer and Information Sciences Department
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Education

- *University of Wisconsin–Madison, Dept. of Comp. Sci., Madison, WI*
  Ph.D. Computer Science 12/2003
  M.S. Computer Science 4/1998
- *Gustavus Adolphus College, St. Peter, MN*
  B.A. Honors Computer Science, *magna cum laude* 4/1996

Employment

- *Google, Inc.*
  Visiting Scientist (while on sabbatical 2013-2014) 9/2013 - present
- *University of Pennsylvania, Dept. of Comp. and Info. Sci., Philadelphia, PA*
  Associate Professor (with tenure) 8/2010 - present
  Assistant Professor 1/2004 - 7/2010
- *University of Wisconsin–Madison, Dept. of Comp. Sci., Madison, WI*
  Research Assistant 6/1997 - 12/2003
  Teaching Assistant (Instructor) 8/1996 - 5/1997
- *IBM Server Development Group, Rochester, MN, USA*
  Intern 6/1998 - 8/1998

Honors, Awards, and Recognitions

- Published over 50 papers (>3500 total citations); PI or Co-PI on 11 U.S. government grants
- *Wired.com*, *Scientific American*, *New Scientist*, and *EE Times* articles highlighting my research
- Four papers selected for IEEE Micro's Annual "Top Picks of Computer Architecture" Issue (2003, 2006, and two in 2012)
- Best Paper Award at HPCA 2012 and ASPLOS 2013 for work on Computational Sprinting
- NSF's Faculty Early Career Development (CAREER) Award, 2007
- Gustavus Adolphus College's *First Decade Outstanding Achievement Award*, 2006
- IBM Graduate Fellowship, 1997-2002

Grants

- NSF *XPS: CLCCA: Improving Parallel Program Reliability Through Novel Approaches to Precise Dynamic Data Race Detection*, CCF-1337174. Co-PI with PI Joe Devietti and Co-PI Steve Zdancewic, $700,000 (four years, September 2013-August 2017).
- NSF CCF *Expeditions in Computer Augmented Program Engineering (ExCAPE): Harnessing Synthesis for Software Design*, CCF-1138996. Co-PI (one of five Penn PI/Co-PIs). Total award: $10M over five years. Penn's portion is $3.75M.
- NSF CCF/SHF *Ultra-Responsive Architectures for Mobile Platforms*, CCF-1161681. PI, $240,000 (four years, May 2012-April 2016). This award is Penn's portion of a $800,000 joint project with three collaborators at University of Michigan.
- NSF *TC: Small: Watchdog: Hardware-Assisted Prevention of All Use-After-Free Security Vulnerabilities*, CNS-1116682. PI with Co-PI Steve Zdancewic. $500,000 (three years, August 2011-July 2014).
- ONR *Ironclad C/C++: Enforcing Memory Safety to Prevent Low-Level Security Vulnerabilities*. PI with Co-PI Steve Zdancewic, $349,000 (three years, May 2011-April 2014).
- DARPA *Echelon: Extreme-scale Compute Hierarchies with Efficient Locality-Optimized Nodes* PI of Penn's subcontract for the NVIDIA-led $9 million UHPC (Ubiquitous High Performance Computing) project, $488,000 (two years, August 2010-August 2012).
- NSF *CCF-SHF: Medium: Formal Analysis of Concurrent Software on Relaxed Memory Models*, CCF-0905464. Co-PI with PI Rajeev Alur, $1,200,000 (four years, July 2009-June 2013).
- NSF *Multicore Bootcamp: REU Supplement*. PI. $16,000 (one year, 2009).
- NSF *CPA-CSA: BLUE CHIP: Security Defenses for Misbehaving Hardware*, CCF-0810947. Co-PI with PI Jonathan Smith, $200,000 (three years, August 2008-July 2011). This award is Penn's half of a joint project with Sam King at University of Illinois.
- DARPA *Terabit Edge Research Activity* Co-PI with PI Jonathan Smith, Department of the Air Force, Sponsor # FA8650-07-C-7743, $270,843 (one year, 2007-2008).
- NSF *CAREER: Semantics and Hardware Implementation of Transactional Memory*, CCF-0644197. PI, $400,000 (five years, June 2007-May 2012).
- NSF *ON-Core: Single-thread Performance via Multi-core Aggregation*, CCF-0541292 Co-PI with PI Amir Roth, $400,000 (three years, May 2006-April 2009).
- Intel Research Grant: *Hardware Support for Memory-Safe C*. PI, $120,000 (three years, 2007-2010).
- Intel Research Grant: *Toward Simpler Multiprocessor Designs*. PI, $120,000 (three years, 2004-2007).
- Sun Microsystems Equipment Grants. PI, 2008 & 2009. T2000 SPARC Server (2008) and SPARC Enterprise T5240 Server (2009), total list price: $53,490

Course Development

- CIS240, 2004 — Redesigned (with E. Lewis) "CIS240: Introduction to Computer Architecture" with the goal of creating a relevant, broad, and exciting course to retain and attract potential majors (this course is required by all CIS-affiliated degrees, including DMD, BAS, BSE, and CE). Our initial experiences with this new course have been extremely positive. Course ratings are high, and many students listed this course as their favorite course on a survey of our CS majors.
- CIS372, 2006 — Overhauled "CIS372: Digital Systems Organization and Design Lab" to create a hands-on lab via replacing simulation-based projects with a design project using actual programmable hardware prototyping boards. Worked with undergraduate TAs to develop the course projects, tutorials, and Verilog code for hardware I/O devices such as a video monitor output and keyboard input. This lab has now been combined into CIS371.
- CIS534, 2010 — Resurrected the parallel programming course, retitled: "CIS534: Multicore Programming and Architecture". The course was updated to include the latest innovations in parallel hardware and techniques for programming such highly parallel hardware.

Courses Taught

Semester	Course	Title	Students	Inst. Rating
Spring 2014	Sabbatical			
Fall 2013	Sabbatical			
Spring 2013	CIS 371	Digital Systems Organization and Design	79	3.42 / 4
Fall 2012	CIS 501	Computer Architecture	128	3.55 / 4
Spring 2012	CIS 371	Digital Systems Organization and Design	59	3.47 / 4
Fall 2011	CIS 501	Computer Architecture	82	3.53 / 4
Spring 2011	CIS 371	Digital Systems Organization and Design	57	3.04 / 4
Fall 2010	CIS 501	Computer Architecture	78	3.11 / 4
Spring 2010	CIS 534	Multicore Programming and Architecture	21	3.63 / 4
Fall 2009	CIS 501	Computer Architecture	37	2.40 / 4
Spring 2009	CIS 371	Digital Systems Organization and Design	40	3.18 / 4
Fall 2008	CIS 501	Computer Architecture	46	3.25 / 4
Spring 2008	CIS 371	Digital Systems Organization and Design	47	3.14 / 4
Fall 2007	Junior sabbatical			
Spring 2007	CIS 372	Digital Systems Organization and Design Lab	43	3.59 / 4
Fall 2006	CIS 240	Introduction to Computer Architecture	89	3.68 / 4
Spring 2006	CIS 372	Digital Systems Organization and Design Lab	32	3.56 / 4
Fall 2005	CIS 501	Computer Architecture	30	3.07 / 4
Spring 2005	CIS 700	Special Topic: Hardware Support for Security	14	3.33 / 4
Fall 2004	CIS 240	Introduction to Computer Architecture	93	3.17 / 4
Spring 2004	CIS 700	Special Topic: Multiprocessor Computer Architecture & Server Workloads	9	3.56 / 4
Average			**55**	**3.33 / 4**

Students, Advising, and Dissertation Committees

PhD Graduates

- Arun Raghavan, 2013
  first employment: Oracle Labs
- Santosh Nagarakatte, 2012
  first employment: Rutgers University
- Colin Blundell, 2010
  Recipient of the 2011 Rubinoff Award (Penn CIS outstanding dissertation award)
  Recipient of IBM Graduate Fellowship (2009-2010)
  first employment: Josef Raviv Memorial Postdoctoral Fellow at IBM Research, 2010-2011
  current employment: Google
- Sebastian Burckhardt (co-advised with Rajeev Alur), 2007
  first employment: Microsoft Research

Current Graduate Students Advised

- Sela Mador-Haim (co-advised with Rajeev Alur), matriculated 2007, completed WPE-I, WPE-II, completed dissertation proposal
- Abhishek Udupa (co-advised with Rajeev Alur), matriculated 2010, completed WPE-I, WPE-II
- Christian DeLozier, matriculated 2010, completed WPE-I, WPE-II
- Laurel Emurian, matriculated 2011

Dissertation Committees

- Jianzhou Zhao (advisor: Steve Zdancewic), 2013
- Adam Aviv (advisors: Jonathan Smith & Matt Blaze), 2012
- Tingting Sha (advisor: Amir Roth), 2011
- Drew Hilton (advisor: Amir Roth), 2010
- Peng Li (advisor: Steve Zdancewic), 2008
- Anne Weinberger Bracy (advisor: Amir Roth), 2008
- Vlad Petric (advisor: Amir Roth), 2007
- Marc Corliss (advisor: E Lewis), 2006

Undergraduate Senior Thesis Projects Supervised

- 2012-2013: Jason Mow, Andrew Braunstein, Nico Mihalich
- 2009-2010: Michajlo Matijkiw
- 2006-2007: Peter Hornyack (2nd place departmental award winner)
- 2005-2006: Joe Devietti, Travis Niedosik

Undergraduate Summer Researchers

- Summer 2009: Andres Velazquez, Evan Benshetler, and Michajlo Matijkiw
- Summer 2006: Peter Hornyack (initially employed by Cisco Systems, now a PhD student at University of Washington)
- Summer 2005: Joe Devietti

Departmental Activities and Service

- Penn Departmental Service
  - Chair Search Committee (2013)
  - Mentoring: Andreas Haeberlen (2010–) and Chris Murphy (2010–)
  - Distinguished Lecture Chair (2011)
  - Computer Engineering Program Committee (2009–), Associate Chair (2010–)
  - Computing Committee (2004–2008)
  - Hiring Committees: Systems (2005 & 2006), Graphics (2011), and Computer Engineering (2012)
  - Space Committee (2004–2007)
  - Graduate Admissions Committee, 2004, 2009–2011
- Penn School of Engineering and Applied Science (SEAS) Service
  - SEAS Computing Committee (2005-2007)

Professional Activities and Service

- Program Committees
  - Top Picks 2014 – IEEE Micro's Top Picks 2014
  - ISCA 2012 – 39th International Symposium on Computer Architecture
  - HPCA 2012 – 18th IEEE Symposium on High Performance Computer Architecture
  - MICRO 2011 – 44th IEEE/ACM International Symposium on Microarchitecture
  - ACSAC 2011 – 27th Annual Computer Security Applications Conference
  - MSPC 2011 – Workshop on Memory Systems Performance and Correctness
  - Top Picks 2011 – IEEE Micro's Top Picks 2011
  - ASPLOS 2011 – 16th Intl. Conf. on Arch. Support for Prog. Lang. and Operating Systems
  - MULTIPROG 2010 – 3rd Workshop on Programmability Issues for Multicore Computers
  - ASPLOS 2010 – 15th Intl. Conf. on Arch. Support for Prog. Lang. and Operating Systems
  - MICRO 2009 – 42nd IEEE/ACM International Symposium on Microarchitecture
  - ICS 2009 – 23rd International Conference on Supercomputing
  - TRANSACT 2009 – 4th ACM SIGPLAN Workshop on Transactional Computing
  - Top Picks 2009 – IEEE Micro's Top Picks 2009
  - ISCA 2008 – 35th International Symposium on Computer Architecture
  - TRANSACT 2008 – 3rd ACM SIGPLAN Workshop on Transactional Computing
  - MULTIPROG 2008 – 1st Workshop on Programmability Issues for Multicore Computers
  - PPoPP 2008 – Symposium on Principles and Practice of Parallel Programming
  - MICRO 2007 – 40th IEEE/ACM International Symposium on Microarchitecture
  - ISCA 2007 – 34th International Symposium on Computer Architecture
  - ISPASS 2007 – International Symposium on Performance Analysis of Systems and Software
  - IPDPS 2007 – The 2007 IEEE International Parallel and Distributed Processing Symposium
  - HiPC 2006 – 13th IEEE International Conference on High Performance Computing
  - ICPP 2006 – The 2006 International Conference on Parallel Processing
  - WMPI 2006 – 4th Workshop on Memory Performance Issues
- Member: ACM (since 1993), IEEE Computer Society (since 1997)
- Previous maintainer of the *WWW Computer Architecture Home Page*, which receives over 100,000 hits a year. (`http://www.cs.wisc.edu/arch/www/`)

Open-Source Software Distributions

- SoftBound, 2009 – `http://www.cis.upenn.edu/acg/softbound/` – SoftBound is a compile-time transformation for enforcing spatial safety of unmodified C code. Softbound was coded primarily by Santosh Nagarakatte as part of a collaborative project with Jianzhou Zhao, Steve Zdancewic, and Milo M. K. Martin.

- FeS_2, 2008 – `http://fes2.cs.uiuc.edu/` – FeS_2 is a full-system execution-driven timing-first micr-simulator for x86. It builds upon Simics, PTLSim, and GEMS's Ruby multiprocessor memory system simulator. FeS_2 itself was developed in a collaboration between Naveen Neelakantam and Craig Zilles from the University of Illinois at Urbana-Champaign and Colin Blundell, Joe Devietti, and Milo M. K. Martin from the University of Pennsylvania.

  - As of Aug. 2009, over three hundred messages have been posted to FeS_2's e-mail list.

- CheckFence, 2007 – `http://checkfence.sourceforge.net/` – CheckFence is a SAT-based formal verification tool that analyzes C code implementing concurrent data types on multiprocessors (concurrent queues, sets etc.) with respect to a selected memory model. Checkfence was created as part of Sebastian Burckhardt's PhD dissertation, which was co-advised by Rajeev Alur and Milo M. K. Martin.

- Multifacet's General Execution-driven Multiprocessor Simulator (GEMS) infrastructure, 2005 – `http://www.cs.wisc.edu/gems/`

  - As of April 2009, over 50 academic papers have used GEMS, 2000 users have registered and downloaded GEMS, and 5000 messages have been posted to the GEMS mailing list.
  - Sun Microsystems created a version of GEMS modified to simulate the best-effort transactional memory of Sun's Rock processor (as mentioned in an article in *EE Times* "Sun rallies industry around Rock CPU" on 01/30/2008).

Patents and Patent Applications

- *Computational Sprinting Using Multiple Cores.* Thomas F. Wenisch, Kevin Pipe, Marios Papaefthymiou, Milo M. K. Martin, and Arun Raghavan. Patent application. PCT/US2012/065654, WO2013075012 A2. Filed November 2011.
- *US 6,981,097: Token based cache-coherence protocol*. Milo M. K. Martin, Mark D. Hill, and David A. Wood. Filed March 2003 / Issued December 2005.
- *US 6,883,070: Bandwidth-adaptive, hybrid, cache-coherence protocol*. Milo M. K. Martin, Daniel J. Sorin, Mark D. Hill, and David A. Wood. Filed November 2001 / Issued April 2005. (Listed in the Microprocessor Report "Patent Watch" column, June 2005)

Court Testimony

- Expert witness testimony regarding the definition of "computer" as defined by the federal Computer Fraud and Abuse Act (CFAA). GWR Medical v. Baez, Civil No. 07-1103, U.S. Federal Court, Eastern District of Pennsylvania, February 12, 2008.

Presentations

Computational Sprinting

- Intel – Hudson, MA – January 2014
- AMD – Austin, TX – June 2012
- Samsung – Austin, TX – June 2012
- Qualcomm – San Diego, CA – August 2012
- NVIDIA – Santa Clara, CA – September 2012
- Qualcomm – Santa Clara, CA – September 2012
- Rutgers University – New Brunswick, NJ – April 2013

Secure Low-Level Programming via Hardware-Assisted Memory-Safe C

- Columbia University – New York, NY – December 2010
- University of Wisconsin – Madison, WI – February 2010
- Microsoft Research – Redmond, WA – December 2009
- VMWare – Palo Alto, CA – November 2009
- Stanford University – Palo Alto, CA – November 2009
- Princeton University – Princeton, NY – October 2009
- University of Texas – Austin, TX – October 2009
- University of Michigan – Ann Arbor, MI – October 2009
- IBM T.J. Watson Research Center – December 2008
- NJ Programming Languages and Systems Seminar (NJPLS) – March 2008

Panel member for Workshop on Exploiting Concurrency Efficiently and Correctly (EC^2) co-located with Computer Aided Verification (CAV) – July 2008

Transactional Memory's Subtle Semantics and Unrestricted Implementation

- Microsoft Research – Redmond, WA – January 2007
- Massachusetts Institute of Technology (MIT) – Cambridge, MA – December 2006
- Intel – Hudson, MA – November 2006
- Princeton University – Princeton, NJ – November 2006
- Intel – Santa Clara, CA – September 2006

Designing Verifiable Multicores: Formal Verification and its Impact on the Snooping versus Directory Protocol Debate

- Intel's Novel Verification and Validation Solution Research Symposium – September 2006
- Invited presentation at the International Conference on Computer Design (ICCD) – October 2005

Panel member of WDDD 2005's panel on deconstructing transactional memory – June 2005

Token Coherence: Decoupling Performance and Correctness

- University of California at Berkeley – Berkeley, CA – April 2003
- Georgia Tech – Atlanta, GA – April 2003
- University of California at San Diego – La Jolla, CA – April 2003
- Duke University – Durham, NC – April 2003

- Carnegie Mellon University – Pittsburgh, PA – April 2003
- University of Illinois – Urbana, IL – March 2003
- University of Pennsylvania – Philadelphia, PA – February 2003
- Northwestern University – Evanston, IL – February 2003
- University of Minnesota – Minneapolis, MN – February 2003
- Intel – Portland, OR – February 2003
- Intel – Santa Clara, CA – February 2003
- Sun Microsystems – Sunnyvale, CA – February 2003

Bandwidth Adaptive Snooping

- Intel & HP/Compaq Joint Seminar – Shrewsbury, MA – September 2002
- HP/Compaq – Marlboro, MA – September 2002
- University of Texas – Austin, TX – December 2001
- IBM Austin Research Lab (ARL) – Austin, TX – December 2001
- University of Minnesota – Minneapolis, MN – September 2001

Publications

Copies of these papers can be found at `http://www.cis.upenn.edu/~milom/`. Citation count data from Google Scholar. In total, my papers have received over 3500 citations.

Author key: *Penn*, Student

Journal Publications

1. *Utilizing Dark Silicon to Save Energy with Computational Sprinting*. *Arun Raghavan*, *Laurel Emurian*, Lei Shao, Marios Papaefthymiou, Kevin P. Pipe, Thomas F. Wenisch, and ***Milo M. K. Martin***. **IEEE Micro**, Volume 33, Number 5, pages 20–28, Sep-Oct 2013.

2. *Hardware-Enforced Comprehensive Memory Safety*. *Santosh Nagarakatte*, ***Milo M K Martin***, *Steve Zdancewic*. **IEEE Micro's "Top Picks of 2012" Issue**, Volume 33, Number 3, May-June 2013. One of 11 papers selected as a top pick from the top architecture conferences of 2012.

3. *Designing for Responsiveness with Computational Sprinting*. *Arun Raghavan*, Yixin Luo, Anuj Chandawalla, Marios Papaefthymiou, Kevin P. Pipe, Thomas F. Wenisch, and ***Milo M. K. Martin***. **IEEE Micro's "Top Picks of 2012" Issue**, Volume 33, Number 3, May-June 2013. One of 11 papers selected as a top pick from the top architecture conferences of 2012.

4. *Why On-Chip Cache Coherence is Here to Stay*. ***Milo M. K. Martin***, Mark D. Hill, Daniel J. Sorin. Communication of the ACM (**CACM**), Vol. 55, Issue 7, pages 78–89, July 2012.

5. *Token Tenure and PATCH: A Predictive/Adaptive Token Counting Hybrid*. *Arun Raghavan*, *Colin Blundell*, and ***Milo M. K. Martin***. ACM Transactions on Architecture and Code Optimization (**ACM TACO**), Vol. 7, No. 2, 31 pages, Article 6, September 2010.

6. *NoSQ: Store-Load Communication without a Store Queue*. *Tingting Sha*, ***Milo M. K. Martin***, and *Amir Roth*, **IEEE Micro's "Top Picks of 2006" Issue**, Volume 27, Number 1, pages 106–113, January-February 2007. One of 11 papers selected as a top pick from the top architecture conferences of 2006.

7. *Subtleties of Transactional Memory Atomicity Semantics*. Colin Blundell, *E Christopher Lewis*, and ***Milo M. K. Martin***, Computer Architecture Letters (**CAL**), Volume 5, Number 2, November 2006.

8. *Token Coherence: A New Framework for Shared-Memory Multiprocessors*. **Milo M. K. Martin**, Mark D. Hill, and David A. Wood, **IEEE Micro's "Top Picks of 2003" Issue**, Volume 23, Number 6, pages 108–116, November-December 2003. One of 15 papers selected as a top pick from the top architecture conferences of 2003.

9. *Simulating a $2M Commercial Server on a $2K PC*. Alaa R. Alameldeen, **Milo M. K. Martin**, Carl J. Mauer, Kevin E. Moore, Min Xu, Daniel J. Sorin, Mark D. Hill and David A. Wood, **IEEE Computer**, Volume 36, Number 2, pages 50–57, February 2003.

10. *Specifying and Verifying a Broadcast and a Multicast Snooping Cache Coherence Protocol*. Daniel J. Sorin, Manoj Plakal, Anne E. Condon, Mark D. Hill, **Milo M. K. Martin** and David A. Wood, IEEE Transactions on Parallel and Distributed Systems (**IEEE TPDS**), Volume 13, Number 6, pages 556–578, June 2002.

Refereed Archival Conference Publications

1. *On-chip Phase Change Heat Sinks Designed for Computational Sprinting*. Lei Shao, Arun Raghavan, *Laurel Emurian*, Marios Papaefthymiou, Thomas Wenisch, Milo Martin, Kevin Pipe. Proceedings of the 30th Annual Thermal Measurement, Modeling, and Management Symposium (**SemiTherm**), March 2014.

2. *WatchdogLite: Hardware-Accelerated Compiler-Based Pointer Checking*. Santosh Nagarakatte, ***Milo M. K. Martin***, *Steve Zdancewic*. Proceedings of the 2014 International Symposium on Code Generation and Optimization (**CGO**), Feb 2014. 29 out of 103 submissions accepted (28%).

3. *Syntax-Guided Synthesis*. *Rajeev Alur*, Rastislav Bodik, Garvit Juniwal, ***Milo M. K. Martin***, *Mukund Raghothaman*, Sanjit A. Seshia, Rishabh Singh, Armando Solar-Lezama, Emina Torlak, *Abhishek Udupa*. Proceedings of the 2013 Formal Methods in Computer-Aided Design (**FMCAD**), October 2013.

4. *Ironclad C++: A Library-Augmented Type-Safe Subset of C++*. *Christian DeLozier*, *Richard Eisenberg*, Santosh Nagarakatte, *Peter-Michael Osera*, ***Milo M. K. Martin***, *Steve Zdancewic*. Proceedings of the 2013 ACM SIGPLAN International Conference on Object Oriented Programming Systems Languages & Applications (**OOPSLA**), pages 287-304, October 2013. 50 out of 189 submissions accepted (26%).

5. *Formal Verification of SSA-Based Optimizations for LLVM*. *Jianzhou Zhao*, *Santosh Nagarakatte*, ***Milo M. K. Martin***, and *Steve Zdancewic*. Proceedings of the 2013 ACM SIGPLAN Conference on Programming Language Design and Implementation (**PLDI**), June 2013. 46 out of 267 submissions accepted (17%).

6. *Transit: Specifying Protocols with Concolic Snippets*. *Abhishek Udupa*, *Arun Raghavan*, *Jyotirmoy V. Deshmukh*, *Sela Mador-Haim*, ***Milo M. K. Martin***, and *Rajeev Alur*. Proceedings of the 2013 ACM SIGPLAN Conference on Programming Language Design an ed Implementation (**PLDI**), June 2013. 46 out of 267 submissions accepted (17%).

7. *Computational Sprinting on a Hardware/Software Testbed*. Arun Raghavan, Laurel Emurian, Lei Shao, Marios Papaefthymiou, Kevin P. Pipe, Thomas F. Wenisch, and ***Milo M. K. Martin***. Proceedings of the 18th Eighteenth International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), March 2013. 44 out of 193 submissions accepted (23%). **Best paper award.**

8. *An Axiomatic Memory Model for POWER Multiprocessors*. Sela Mador-Haim, Luc Maranget, Susmit Sarkar, Kayvan Memarian, Jade Alglave, Scott Owens, *Rajeev Alur*, ***Milo M. K. Martin***, Peter Sewell, and Derek Williams. Proceedings of Computer Aided Verification (**CAV**), July 2012. 58 out of 185 submissions accepted (31%).

9. *Watchdog: Hardware for Safe and Secure Manual Memory Management and Full Memory Safety*. Santosh Nagarakatte, ***Milo M. K. Martin***, and *Steve Zdancewic*. Proceedings of the 39th ACM International Symposium on Computer Architecture (**ISCA**), June 2012. 47 out of 262 submissions accepted (18%).

10. *Multicore Acceleration for Priority Based Schedulers for Concurrency Bug Detection*. Santosh Nagarakatte, Sebastian Burckhardt, ***Milo M. K. Martin***, Madan Musuvathi. Proceedings of the 2012 ACM SIGPLAN Conference on Programming Language Design and Implementation (**PLDI**), June 2012. 48 out of 255 submissions accepted (19%).

11. *Computational Sprinting*. Arun Raghavan, Yixin Luo, Anuj Chandawalla, Marios Papaefthymiou, Kevin P. Pipe, Thomas F. Wenisch, and ***Milo M. K. Martin***. Proceedings of the 18th Symposium on High Performance Computer Architecture (**HPCA**), Feb 2012. 36 of 210 submissions accepted (17%). **Best paper award.**

12. *Formalizing the LLVM Intermediate Representation for Verified Program Transformations*. Jianzhou Zhao, Santosh Nagarakatte, ***Milo M. K. Martin***, and *Steve Zdancewic*. Proceedings of the 39th ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages (**POPL**), Jan 2012. 44 of 205 submissions accepted (21%).

13. *Litmus Tests for Comparing Memory Consistency Models: How Long Do They Need to Be?*. Sela Mador-Haim, *Rajeev Alur*, ***Milo M. K. Martin***. Proceedings of the 48th Design Automation Conference (**DAC**), June 2011. 156 of 690 submissions accepted (23%).

14. *Generating Litmus Tests for Contrasting Memory Consistency Models*. Sela Mador-Haim, *Rajeev Alur*, ***Milo M. K. Martin***. Proceedings of Computer-aided Verification (**CAV**), July 2010. 51 of 145 submissions accepted (35%).

15. *RetCon: Transactional Repair without Replay*. Colin Blundell, Arun Raghavan, and ***Milo M. K. Martin***. Proceedings of the 37th International Symposium on Computer Architecture (**ISCA**), June 2010. 44 of 245 submissions accepted (18%).

16. *CETS: Compiler Enforced Temporal Safety for C*. Santosh Nagarakatte, Jianzhou Zhao, ***Milo M. K. Martin***, and *Steve Zdancewic*. Proceedings of ACM SIGPLAN International Symposium on Memory Management (**ISMM**), June 2010. 13 out of submissions 30 accepted (43%).

17. *Overcoming an Untrusted Computing Base: Detecting and Removing Malicious Hardware Automatically*. Matthew Hicks, Murph Finnicum, Samuel T. King, ***Milo M. K. Martin***, and *Jonathan M. Smith*. Proceedings of the 31st IEEE Symposium on Security & Privacy (**S&P**), May 2010. 26 of 237 submissions accepted (11%).

18. *InvisiFence: Performance-Transparent Memory Ordering in Conventional Multiprocessors*. Colin Blundell, ***Milo M. K. Martin***, and Tom Wenisch. Proceedings of the 36th International Symposium on Computer Architecture (**ISCA**), pages 233–244, June 2009. 43 of 210 submissions accepted (20%).

19. *SoftBound: Highly Compatible and Complete Spatial Memory Safety for C*. Santosh Nagarakatte, Jianzhou Zhao, ***Milo M. K. Martin***, and *Steve Zdancewic*. Proceedings of ACM SIGPLAN Conference on Programming Language Design and Implementation (**PLDI**), pages 245–258 June 2009. 41 of 196 submissions accepted (21%).

20. *Token Tenure: PATCHing Token Counting Using Directory-Based Cache Coherence*. Arun Raghavan, Colin Blundell, and ***Milo M. K. Martin***. Proceedings of the 41st International Symposium on Microarchitecture (**MICRO**), pages 47–58, November 2008. 40 of 210 submissions accepted (19%).

21. *HardBound: Architectural Support for Spatial Safety of the C Programming Language*. Joe Devietti, Colin Blundell, ***Milo M. K. Martin***, and *Steve Zdancewic*. Proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), pages 103–114, March 2008. 31 of 127 submissions accepted (24%).

22. *Making the Fast Case Common and the Uncommon Case Simple in Unbounded Transactional Memory*. Colin Blundell, Joe Devietti, *E Christopher Lewis*, and ***Milo M. K. Martin***. Proceedings of the 34th International Symposium on Computer Architecture (**ISCA**), pages 24–34, June 2007. 46 of 204 submissions accepted (23%).

23. *CheckFence: Checking Consistency of Concurrent Data Types on Relaxed Memory Models*. Sebastian Burckhardt, *Rajeev Alur*, and ***Milo M. K. Martin***. Proceedings of the ACM SIGPLAN Conference on Programming Language Design and Implementation (**PLDI**), pages 12–21, June 2007. 45 of 178 submissions accepted (25%).

24. *NoSQ: Store-Load Communication without a Store Queue*. Tingting Sha, ***Milo M. K. Martin***, and *Amir Roth*. Proceedings of the 39th International Symposium on Microarchitecture (**MICRO**), pages 285–296, December 2006. 42 of 174 submissions accepted (24%).

25. *Bounded Model Checking of Concurrent Data Types on Relaxed Memory Models: A Case Study*. Sebastian Burckhardt, *Rajeev Alur*, and ***Milo M. K. Martin***. Proceedings of Computer-aided Verification (**CAV**), pages 489–502, August 2006. 35 of 121 regular submissions accepted (29%).

26. *Scalable Store-Load Forwarding via Store Queue Index Prediction*. Tingting Sha, ***Milo M. K. Martin***, and *Amir Roth*. Proceedings of the 38th International Symposium on Microarchitecture (**MICRO**), pages 159–170, November 2005. 29 of 147 submissions accepted (20%).

27. *Formal Verification and its Impact on the Snooping versus Directory Protocol Debate*. ***Milo M. K. Martin***. Proceedings of the International Conference on Computer Design (**ICCD**), pages 543–449, October 2005. **Invited Paper.** 101 of 313 non-invited submissions accepted (32%).

28. *Improving Multiple-CMP Systems Using Token Coherence*. Michael R. Marty, Jesse D. Bingham, Mark D. Hill, Alan J. Hu, ***Milo M. K. Martin***, and David A. Wood. Proceedings of the International Symposium on High Performance Computer Architecture (**HPCA**), pages 328–339, February 2005. 28 of 181 submissions accepted (15%).

29. *Verifying Safety of a Token Coherence Implementation by Parametric Compositional Refinement*. Sebastian Burckhardt, *Rajeev Alur*, and ***Milo M. K. Martin***. Sixth International Conference on Verification, Model Checking and Abstract Interpretation (**VMCAI**), pages 130–145, January 2005. 27 of 92 submissions accepted (29%).

30. *Using Speculation to Simplify Multiprocessor Design*. Daniel J. Sorin, ***Milo M. K. Martin***, Mark D. Hill, and David A. Wood, Proceedings of the 18th International Parallel and Distributed Processing Symposium (**IPDPS**), pages 75–84, April 2004. 142 of 447 submissions accepted (32%).

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33. *SafetyNet: Improving the Availability of Shared Memory Multiprocessors with Global Checkpoint/Recovery*. Daniel J. Sorin, **Milo M. K. Martin**, Mark D. Hill, and David A. Wood. Proceedings of the 29th International Symposium on Computer Architecture (**ISCA**), pages 123–134, May 2002. 27 of 180 submissions accepted (15%).

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36. *Timestamp Snooping: An Approach for Extending SMPs*. **Milo M. K. Martin**, Daniel J. Sorin, Anastassia Ailamaki, Alaa R. Alameldeen, Ross M. Dickson, Carl J. Mauer, Kevin E. Moore, Manoj Plakal, Mark D. Hill, and David A. Wood. Proceedings of the 9th International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), pages 25–36, November 2000. 24 of 114 submissions accepted (21%).

37. *Exploiting Dead Value Information*. **Milo M. Martin**, Amir Roth, and Charles Fischer. Proceedings of the 30th Annual International Symposium on Microarchitecture (**MICRO**), pages 125–135, December 1997. 35 of 103 submissions accepted (34%).

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1. *MAMA: Mostly Automatic Management of Atomicity*. *Christian DeLozier*, *Joseph Devietti*, and ***Milo M. K. Martin***. 5th Workshop on Determinism and Correctness in Parallel Programming (WoDet), March 2014.

2. *Overcoming an Untrusted Computing Base: Detecting and Removing Malicious Hardware Automatically*. Matthew Hicks, Murph Finnicum, Samuel T. King, ***Milo M. K. Martin***, and *Jonathan M. Smith*. USENIX ;login:, Vol. 35, Number 6, pages 31-41, December 2010.

3. *Securing Hardware Platforms Against Malicious Through Static Analysis*. Matthew Hicks, Samuel T. King, ***Milo M. K. Martin***, and *Jonathan M. Smith*. ACM Symposium on Operating Systems Principles Work In Progress Session, Oct 2009

4. *Specifying Relaxed Memory Models for State Exploration Tools*. *Sela Mador-Haim*, *Rajeev Alur*, and ***Milo M. K. Martin***. Position paper for the workshop on (EC)2: Exploiting Concurrency Efficiently and Correctly, June 2009

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7. *Deconstructing Transactional Semantics: The Subtleties of Atomicity*. *Colin Blundell*, *E Christopher Lewis*, and ***Milo M. K. Martin***. Workshop on Duplicating, Deconstructing, and Debunking (**WDDD**), June 2005.

8. *Evaluating Non-deterministic Multi-threaded Commercial Workloads*. Alaa R. Alameldeen, Carl J. Mauer, Min Xu, Pacia J. Harper, **Milo M. K. Martin**, Daniel J. Sorin, Mark D. Hill and David A. Wood. Workshop On Computer Architecture Evaluation using Commercial Workloads (**CAECW**), February 2002.

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1. *Terabit Edge Research Activity (TERA). J. M. Smith* and ***Milo M. K. Martin***, Technical Report AFRL-RY-WP-TR-2008-1254, Air Force Research Laboratory, October 2008.

2. *Unrestricted Transactional Memory: Supporting I/O and System Calls within Transactions*. *Colin Blundell*, *E Christopher Lewis*, and ***Milo M. K. Martin***, Technical Report CIS-06-09, Department of Computer and Information Science, University of Pennsylvania, Philadelphia, PA, April 2006.

3. *Fast Checkpoint/Recovery to Support Kilo-Instruction Speculation and Hardware Fault Tolerance*. Daniel J. Sorin, **Milo M. K. Martin**, Mark D. Hill, and David A. Wood, Technical Report CS-TR-2000-1420, Dept. of Computer Sciences, University of Wisconsin, Madison, WI, October 2000.

Media

- "Computational Sprinting"
  - Your Future iPhone May Be Stuffed With Wax, *Wired.com*, August 23, 2013

  - Computational sprinting with wax takes heat off smartphones, *PhysOrg.com*, August 27, 2013.
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  - Could "Computational Sprinting" Speed Up Smart Phones without Burning Them Out?, *Scientific American*, February 29, 2012.
  - Researchers propose "overclock" scheme for mobiles; Processing at a sprint to overcome tech limitations, *The Register*, February 21, 2012.
  - Researchers Propose "Computational Sprinting" To Speed Up Chips By 1000% — But Only For A Second, *TechCrunch*, February 28, 2012
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- "Why Cache Coherence is Here to Stay"
  - Research consortium claims solution for multi-core scaling, *EE Times*, April 16, 2012.
- Quoted in the *MIT Technology Review* article "Intel's New Strategy: Power Efficiency", June 2006 (`http://www.techreview.com/printer_friendly_article.aspx?id=16943`)

Miscellaneous Information

- U.S. Citizen
- Erdos number: 3 (Paul Erdos to Michael Saks to Anne Condon to me)